AMENDMENTS TO THE SPECIFICATION:

Please replace from page 2, line 2, through page 8, line 8, with the following new replacement paragraphs:

There has been conventionally known a liquid crystal display device driven by an active matrix manner, as one type of display devices. Note that, the present specification describes a liquid crystal display device as an example of the display device according to the present invention; however, the present invention is not limited to this kind of display device but may be used for other types of display device.

As shown in Figure 10, the active-matrix type liquid crystal display device includes an pixel array ARY, and a scanning signal line driving circuit GD and a data signal

line driving circuit SD.

The pixel array ARY includes a plurality of scanning signal lines GL (1) through GL (j) and a plurality of data signal lines SL (1) through SL (i) intersecting with each other, and each compartment defined by two adjacent scanning signal lines GL (hereinafter referred to as GL to specify an arbitrary one, or also as a generic name) and two adjacent data signal lines SL (hereinafter referred to as SL to specify an arbitrary one, or also as a generic name) is provided with a pixel PIX. Thus, the pixels PIX are disposed in a matrix manner.

The data signal line driving circuit SD mainly includes a shift register and a sampling circuit, and is supplied with a start pulse signal SSP and a clock signal SCK as control signals from an external circuit (not shown), which also supplies an image signal VIDEO to the data signal line driving circuit SD. When the start pulse SSP is supplied, the data signal line driving circuit SD samples the supplied image signal VIDEO in synchronism with the clock signal SCK by using the clock signal as a timing signal, and then amplifies the image signal as required before writing it into the data signal lines SL (1) through SL (i).

The scanning signal line driving circuit GD mainly includes a shift register, and is supplied with a start

pulse GSP and a clock signal GCK as control signals from an external circuit (not shown). When the start pulse signal GSP is supplied, the scanning signal line driving circuit GD drives the scanning signal lines GL (1) through GL(j) by sequentially selecting these signal lines in synchronism with the clock signal GCK by using the clock signal as a timing signal. With this operation, a switching element (described later) provided in the pixel PIX is turned on or off, so that the image signal (data) written in the data signal line SL is written to the pixel PIX, and is held in the pixel PIX.

With such a display device, the applicant of the present invention has proposed a technique in which at least one of the data signal line driving circuit SD and the scanning signal line driving circuit GD is constituted of a plurality of driving circuits, which are driven either independently or together (see Patent Publication 1).

With this technique, it is possible to switch the driving circuits for driving the pixel array, according to the type of supplied image or the usage environment. This enables image display with an optimal display format. Power consumption can be reduced as well.

For example, in case of carrying out both monochrome display and color display with a single display device, monochrome display is performed by

processing monochrome data by a processing circuit for color display. However, in this manner, monochrome display consumes the same quantity of power as that for color display, and therefore there are no advantages in carrying out monochrome display. This can be overcome by the arrangement in which a plurality of driving circuits is provided. By separately installing driving circuits for monochrome display and color display, power consumption can be reduced to that only required for the monochrome display.

Further, a plurality of driving circuits enables overwriting of images by performing writing of image signals with some time differences, thus realizing superimpose display without externally processing the image signals.

[Patent Publication 1]

Japanese Laid-Open Patent Publication, *Tokukai* 2002-32048 (published on January 31, 2002)

[PROBLEMS TO BE SOLVED BY THE INVENTION]

As described above, the applicant of the present invention has proposed a structure in which a data signal line driving circuit or a scanning signal line driving circuit is constituted of a plurality of driving circuits which are driven either independently or together.

As a possible modification, this structure could be

arranged so that one of the plurality of driving circuits are supplied with two-systems of clock signals, and the remaining driving circuits are supplied with one system of clock signals, for example.

More specifically, for example, in an arrangement in which two data signal line driving circuits are provided on both ends of the data signal lines by being connected to each other via the data signal lines, one of the data signal line driving circuits includes two-systems of shift registers and uses two-systems of clock signals for each shift register, while the other data signal line driving circuit includes only one system of shift register and uses only one of the two systems of clock signals.

In this case, to simplify the structure of an external interface, the clock signal to be shared by the two data signal line driving circuits is supplied in common to these data signal line driving circuits. However, in this case, there arises a shift in the sampling timing of image signal in the data signal line driving circuit using two systems of clock signals. This causes a problem of deterioration of display quality.

Such shifting is caused by a difference of wiring loads due to the different routing of the wirings supplying the two-systems of clock signals. More specifically, as shown in Figure 11, a first clock signal ck1 is supplied to

both a first data signal line driving circuit SD1 provided on the side of a signal input section 103, and a second data signal line driving circuit SD2 provided on the opposite end, while a second clock signal ck2 is supplied only to the first data signal line driving circuit SD1. A wiring 100 for the first clock signal ck1 supplied to both of the first and second data signal driving circuits SD1 and SD2 is longer than a wiring 101 for the second clock signal ck2 supplied only to the first data signal line driving circuit SD1. The wiring 100 therefore has a greater wiring load than the wiring 101, and accordingly the wiring load is different between the wiring 100 and wiring 101.

As shown in Figure 12, assuming that the wiring 100 and the wiring 101 are respectively supplied with the first clock signal ck1 and the second clock signal ck2 opposite in phase to each other. In this case, the first clock signal ck1 supplied to the wiring 100 with greater wiring load gets behind of the second clock signal ck2. Accordingly, even when the wiring 100 and the wiring 101 are at substantially the same distance from the signal input section 103, the phase relation between the first clock signal ck1 supplied through the wiring 100 and the second clock signal ck2 supplied through the wiring 101 changes. In the data signal line driving circuit SD1, the

change of phase relation between the respective clock signals causes a shift in the sampling timing of the image signal.

As one possible solution for such a case, the respective clock signals ck1 and ck2 could be adjusted beforehand in an external circuit where the respective clock signals are created, so as to cancel such a phase difference due to the difference in wiring load between the wiring 100 and the wiring 101.

However, when the value of correction time is 25 ns for example, the external circuit requires a source clock (system clock) of not less than 20 Mhz, and causes an increase of power consumption. In recent years, the foregoing display devices have been often used for mobile devices, and therefore, the source clock tends to be reduced for realizing low power consumption. Therefore, there are some difficulties to adopt the foregoing technique of correcting the phase difference in the external circuit.

Further, in case of a liquid crystal display device, the wiring load tend to depend on a capacitance formed by the wiring, a counter electrode, and a liquid crystal layer (dielectric substance) which is held between the wiring and the counter electrode. Therefore, the wiring load also changes depending on the material or thickness of

the liquid crystal layer, and if the difference were to be corrected by an external circuit, correction level have to be adjusted for each display panel, thus increasing costs.